

What is claimed is:

1 1. A sequential pulse train generator consists of
2 thin-film transistors, comprising:
3 a first and second dynamic shift register circuit, each
4 of which has a first, second, third, fourth, and
5 fifth input terminal, and a first and second
6 output terminal, first, second, third and fourth
7 input terminal of the first dynamic shift
8 register circuit coupled to receive an initial
9 pulse train, the inverted initial pulse train, a
10 clock signal and the inverted clock signal, the
11 fifth input terminal of the first dynamic shift
12 register circuit coupled to the first input
13 terminal of the second dynamic shift register
14 circuit, the third and fourth input terminal of
15 the second dynamic shift register circuit coupled
16 to receive the inverted clock signal and the
17 clock signal, respectively;
18 a first and second level shifter, each of which has a
19 first and second input terminal, and an output
20 terminal, the first and second input terminal of
21 the first level shifter coupled to the first and
22 second output terminal of the first dynamic shift
23 register circuit, the output terminal of the
24 first level shifter coupled to the first output
25 terminal of the first dynamic shift register
26 circuit, the first and second input terminal of
27 the second level shifter coupled to the first and

28 second output terminal of the second dynamic
29 shift register circuit, the output terminal of
30 the second level shifter coupled to the first
31 output terminal of the second dynamic shift
32 register circuit, respectively; and
33 a first and second inverter having output terminals
34 coupled to the output terminals of the first and
35 second level shifter, and outputting a first and
36 second sequential pulse train, the output
37 terminal of the first inverter coupled to the
38 second input terminal of the second dynamic shift
39 register circuit,
40 wherein the amplitude of the clock signal is not larger
41 than half the amplitude of the output signal of
42 the inverter.

1 2. The sequential pulse train generator as claimed in
2 claim 1, wherein each of the first and second dynamic shift
3 register circuit comprises:
4 a first transistor of a first type having a gate
5 coupled to the first input terminal and a drain
6 coupled to the second input terminal;
7 a second transistor of a second type having a gate
8 coupled to the second input terminal and a source
9 coupled to receive a first voltage;
10 a third transistor of the second type having a gate
11 coupled to the first input terminal, a drain
12 coupled to the fifth input terminal and a source
13 coupled to a drain of the second transistor;

14 a fourth transistor of the second type having a gate
15 coupled to the source of the third transistor, a
16 drain coupled to a source of the first transistor
17 and a source coupled to receive the first
18 voltage;
19 a fifth transistor of the second type having a gate
20 coupled to the source of the first transistor, a
21 drain coupled to the third input terminal and a
22 source coupled to the first output terminal;
23 a sixth transistor of the second type having a gate
24 coupled to the second input terminal, a drain
25 coupled to the source of the fifth transistor and
26 a source coupled to receive the first voltage;
27 and
28 a seventh transistor of the second type having a gate
29 coupled to the gate of the fifth transistor, a
30 drain coupled to the fourth input terminal and a
31 source coupled to the second output terminal.

1 3. The sequential pulse train generator as claimed in
2 claim 2, wherein each of the first and second level shifters
3 comprise:
4 an eighth transistor of the first type having a gate
5 coupled to receive the first voltage and a source
6 coupled to receive a second voltage;
7 a ninth transistor of the first type having a coupled
8 gate and drain, and a source coupled to a drain
9 of the eighth transistor;
10 a tenth transistor of the first type having a gate
11 coupled to gate of the ninth transistor, a source

12 coupled to receive the second voltage and a drain
13 coupled to the output terminal;
14 an eleventh transistor of the second type having a gate
15 coupled to the drain of the eighth transistor, a
16 source coupled to the drain of the ninth
17 transistor and a drain coupled to the first input
18 terminal; and
19 a twelfth transistor of the second type having a gate
20 coupled to the gate of the eleventh transistor, a
21 source coupled to the drain of the tenth
22 transistor and a source coupled to the second
23 input terminal.

1 4. The sequential pulse train generator as claimed in
2 claim 2, wherein each of the first and second dynamic shift
3 register circuit further comprises a capacitor coupled
4 between the gate and source of the fifth transistor.

1 5. The sequential pulse train generator as claimed in
2 claim 3, wherein the first type is P type and the second
3 type is N type.

1 6. The sequential pulse train generator as claimed in
2 claim 3, wherein the first voltage is a ground voltage and
3 the second voltage is not less than 7 volt.

1 7. The sequential pulse train generator as claimed in
2 claim 1, wherein amplitude of the clock signal is lower than
3 4 volt.

1 8. A sequential pulse train generator consists of
2 thin-film transistors, comprising:

3 a first, second and third dynamic shift register
4 circuit, each of which has a first, second,
5 third, and fourth input terminal, and a first and
6 second output terminal, the first, second and
7 third input terminal of the first dynamic shift
8 register circuit coupled to receive an initial
9 pulse train, the inverted initial pulse train and
10 a clock signal, the fourth input terminal of the
11 first dynamic shift register circuit coupled to
12 the second input terminal of the third dynamic
13 shift register circuit, the third input terminal
14 of the second dynamic shift register circuit
15 coupled to receive the inverted clock signal, the
16 third input terminal of the third dynamic shift
17 register circuit coupled to receive the clock
18 signal;
19 a first, second and third level shifter, each of which
20 has a first and second input terminal, and an
21 output terminal, the first and second input
22 terminal of the first level shifter coupled to
23 the first and second output terminal of the first
24 dynamic shift register circuit, the first and
25 second input terminal of the second level shifter
26 coupled to the first and second output terminal
27 of the second dynamic shift register circuit, the
28 first and second input terminal of the third
29 level shifter coupled to the first and second
30 output terminal of the third dynamic shift
31 register circuit; and

32 a second, third, fourth, fifth, sixth and seventh
33 inverter, input terminals of the second, third
34 and fourth inverter coupled to the output
35 terminals of the first, second and third level
36 shifter, output terminals of the second and third
37 inverter coupled to the first input terminals of
38 the second and third dynamic shift register
39 circuit, input terminals of the fifth, sixth and
40 seventh inverter coupled to the output terminals
41 of the second, third and fourth inverter, an
42 output terminal of the fifth inverter coupled to
43 the second input terminal of the second dynamic
44 shift register circuit, the output terminals of
45 the fifth, sixth and seventh inverter outputting
46 a first, second and third sequential pulse train,
47 respectively,
48 wherein the amplitude of the clock signal is not larger
49 than half the amplitude of the output signal of
50 the inverter..

1 9. The sequential pulse train generator as claimed in
2 claim 8, wherein each of the first, second and third dynamic
3 shift register circuits comprise:

4 a first transistor of a first type having a gate
5 coupled to the first input terminal, a drain
6 coupled to the second input terminal and a source
7 coupled to the third output terminal;
8 a second transistor of a second type having a gate
9 coupled to the fourth input terminal, a source

10 coupled to receive a first voltage and a drain
11 coupled to the third output terminal;
12 a third transistor of the second type having a gate
13 coupled the second output terminal, a drain
14 coupled to the third input terminal and a source
15 coupled to the first output terminal; and
16 a fourth transistor of the second type having a gate
17 coupled to the second input terminal, a drain
18 coupled to the first output terminal and a source
19 coupled to receive the first voltage.

1 10. The sequential pulse train generator as claimed in
2 claim 9, wherein each of the first, second and third level
3 shifters comprise:

4 a fifth transistor of the first type having a gate
5 coupled to receive the first voltage and a source
6 coupled to receive a second voltage;
7 a sixth transistor of the first type having a gate
8 coupled to a drain of the fifth transistor and a
9 drain coupled to the output terminal;
10 a seventh transistor of the second type having a gate
11 coupled to receive the second voltage, a source
12 coupled to the first input terminal and a drain
13 coupled to the output terminal; and
14 a first inverter having an input terminal coupled to
15 the second input terminal and an output terminal
16 coupled to the gate of the sixth transistor.

1 11. The sequential pulse train generator as claimed in
2 claim 9, wherein each of the first, second and third dynamic

3 shift register circuits further comprise a capacitor coupled
4 between the gate and source of the third transistor.

1 12. The sequential pulse train generator as claimed in
2 claim 10, wherein the first type is P type and the second
3 type is N type.

1 13. The sequential pulse train generator as claimed in
2 claim 10, wherein the first voltage is a ground voltage and
3 the second voltage is not less than 7 volt.

1 14. The sequential pulse train generator as claimed in
2 claim 8, wherein amplitude of the clock signal is lower than
3 4 volt.

1 15. A sequential pulse train generator consists of
2 thin-film transistors, comprising:
3 a first, second and third dynamic shift register
4 circuit, each of which has a first, second and
5 third input terminal, and a first and second
6 output terminal, the first and second input
7 terminal of the first dynamic shift register
8 circuit coupled to receive an initial pulse train
9 and a clock signal, the third input terminal of
10 the first dynamic shift register circuit coupled
11 to the first input terminal of the third dynamic
12 shift register circuit, the second input terminal
13 of the second dynamic shift register circuit
14 coupled to receive the inverted clock signal, the
15 second input terminal of the third dynamic shift

16 register circuit coupled to receive the clock
17 signal;
18 a first, second and third level shifter, each of which
19 has a first and second input terminal, and an
20 output terminal, the first and second input
21 terminal of the first level shifter coupled to
22 the first and second output terminal of the first
23 dynamic shift register circuit, the first and
24 second input terminal of the second level shifter
25 coupled to the first and second output terminal
26 of the second dynamic shift register circuit, the
27 first and second input terminal of the third
28 level shifter coupled to the first and second
29 output terminal of the third dynamic shift
30 register circuit; and
31 a first, second and third buffer, input terminals of
32 the first, second and third buffer coupled to the
33 output terminals of the first, second and third
34 level shifter, output terminals of the second
35 buffer coupled to the third input terminal of the
36 first dynamic shift register circuit and to the
37 first input terminal of the third dynamic shift
38 register circuit;
39 wherein the amplitude of the clock signal is not larger
40 than half the amplitude of the output signal of
41 the inverter.